

Please amend the above-captioned application to read as shown below.

In the claims

Please amend Claim 16 as shown below.

1. (Cancelled)
2. (Previously Amended) The device as in Claim 56, wherein the packaged semiconductor is packaged in a ball grid array package.
3. (Previously Amended) The device as in Claim 56, wherein the unpackaged semiconductor die is a graphics-processor.
4. (Previously Amended) The device as in Claim 56, wherein the packaged semiconductor is a memory.
5. (Previously Amended) The device as in Claim 56, wherein a plurality of packaged semiconductors are attached to the package module.
6. (Previously Amended) The device as in Claim 56, wherein the unpackaged semiconductor die is wire bonded to the package module.
7. (Withdrawn)
8. (Previously Amended) The device as in Claim 56, wherein attached includes surface-mount technology reflow.
9. (Previously Amended) The device as in Claim 56, wherein the encapsulated structure has a footprint greater than the footprint of the unpackaged semiconductor die.
10. (Withdrawn)
11. (Previously Amended) The device as in Claim 56, wherein the footprint size of the package module is one of 35 mm × 35 mm, 31 mm × 31 mm, 27 mm × 27 mm, 37.5 mm × 37.5 mm, 40 mm × 40 mm, 42 mm × 42 mm, or 42.5 mm × 42.5 mm.
12. (Withdrawn)

13. (Withdrawn)
14. (Withdrawn)
15. (Cancelled)
16. (Previously Amended) The device as in Claim 56, wherein the packaged semiconductor die is packaged in a ball grid array package.
17. (Previously Amended) The device as in Claim 57, wherein a plurality of packaged memory are attached to the package module.
18. (Previously Amended) The device as in Claim 57, wherein directly attached includes the graphics processing die being wire bonded to the package module.
19. (Withdrawn)
20. (Previously Amended) The device as in Claim 57, wherein attached includes surface-mount technology reflow.
21. (Previously Cancelled)
22. (Withdrawn)
23. (Previously Amended) The device as in Claim 57, wherein the standard package sizes include one of 35 mm x 35 mm, 31 mm x 31 mm, 27 mm x 27 mm, 37.5 mm x 37.5 mm, 40 mm x 40 mm, 42 mm x 42 mm, or 42.5 mm x 42.5 mm.
24. (Withdrawn)
25. (Withdrawn)
26. (Withdrawn)
27. (Withdrawn)
28. (Withdrawn)
29. (Withdrawn)

30. (Withdrawn)

31. (Withdrawn)

32. (Withdrawn)

33. (Withdrawn)

34. (Withdrawn)

35. (Withdrawn)

36. (Withdrawn)

37. (Withdrawn)

38. (Withdrawn)

39. (Withdrawn)

40. (Withdrawn)

41. (Previously Cancelled)

42. (Previously Cancelled)

43. (Previously Cancelled)

44. (Previously Amended) The multi-die module as in Claim 58, further including a second packaged semiconductor die mounted on the first surface of the substrate.

45. (Previously Amended) The multi-die module as in Claim 58, further including a plurality of unpackaged semiconductor die mounted on the first surface of the substrate.

46. (Previously Amended) The multi-die module as in Claim 58, wherein the unpackaged semiconductor die is mounted to the first surface of the substrate by wire bonding.

47. (Previously Amended) The multi-die module as in Claim 58, wherein the encapsulating structure is further comprised of an encapsulating material including epoxy, metal cap or silicon coatings.

48. (Withdrawn)
49. (Previously Cancelled)
50. (Withdrawn)
51. (Withdrawn)
52. (Withdrawn)
53. (Previously Amended) The multi-die module as in Claim 58, wherein the  
unpackaged semiconductor die is a graphics processor.

54. (Previously Amended) The multi-die module as in Claim 58, wherein the  
packaged semiconductor die is a memory.

55. (Withdrawn)

56. (Previously Added) A device comprising:

a package module including a substrate having a standard package footprint;  
an unpackaged semiconductor die directly attached to the package module, the  
unpackaged semiconductor die encapsulated onto the package module in a structure  
having a planar top surface; and  
a packaged semiconductor die having a top surface and attached to the package  
module;

wherein the planar top surface of the encapsulated structure and the top surface of  
the packaged semiconductor die are of equal distance from the substrate.

57. (Previously Added) A device comprising:  
a package module sized to be interchangeable with standard package sizes;

a graphics-processing die directly attached to the package module, the graphics-processing die encapsulated on the package module in a structure having a planar top surface; and

a packaged memory die having a top surface and attached to the package module; wherein the planar top surface of the encapsulated structure and the top surface of the packaged memory die are of equal distance from the package module.

58. (Previously Added) A multi-die module, comprising:

a substrate having a first surface and a second surface;  
an unpackaged semiconductor die mounted to the first surface of the substrate, the semiconductor die encapsulated in a structure having a planar top surface; and  
a packaged semiconductor die having a top surface and mounted on the first surface of the substrate;

wherein the planar top surface of the encapsulated structure and the top surface of the packaged semiconductor die are of equal distance from the substrate.

59. (Previously Added) A multi-die module, comprising:

a substrate having a first surface;  
an unpackaged semiconductor die mounted to the first surface of the substrate, the semiconductor die encapsulated in a structure; and  
a packaged semiconductor die mounted on the first surface of the substrate  
wherein the encapsulating structure is further comprised of an encapsulating material of a metal cap.

60. (New) The device of claim 56 further including a planar heat sink adapted to engage the encapsulated structure and the top surface of the packaged semiconductor.